

The Junction Transistor

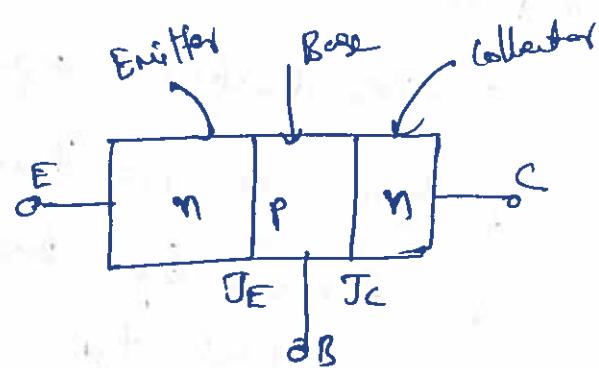
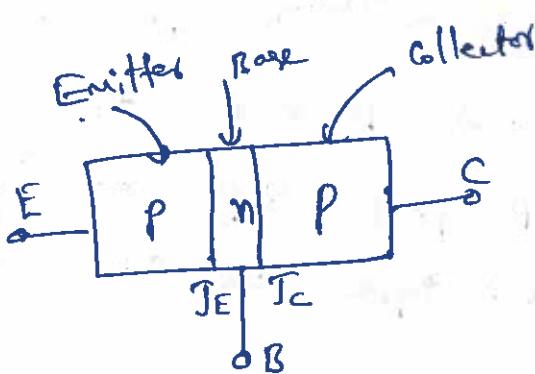
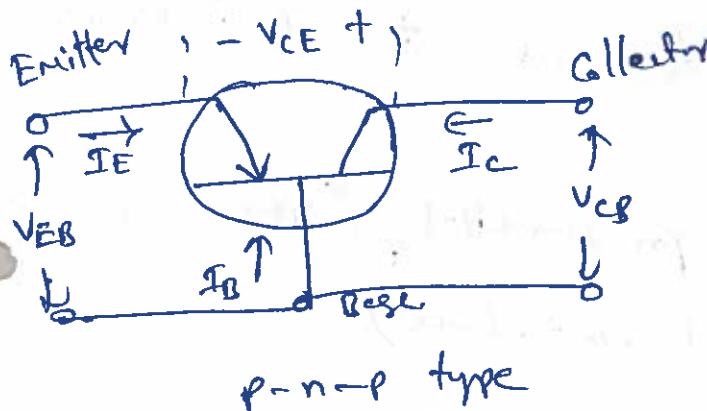
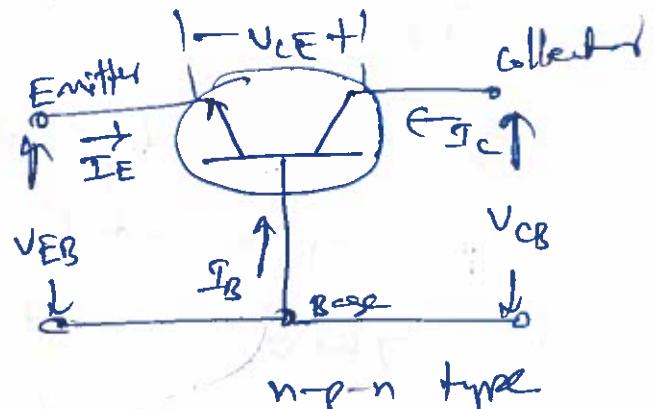


Fig: ~~p-n-p and n-p-n transistor~~



p-n-p type



n-p-n type

Fig: Circuit representation of the two types

when a third doped element is added to a p-n junction diode in such a way that two p-n junctions are formed. The resulting device is known as a transistor.

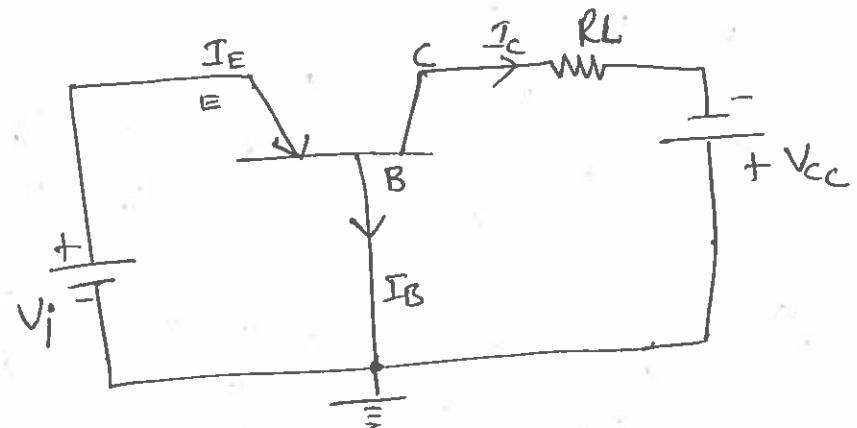
Transistor consists of two p-n junctions formed by sandwiching either p-type or n-type semiconductor between a pair of opposite types. They are two types of transistors. These are (a) n-p-n transistor and p-n-p

n-p-n transistor is composed of two n-type semiconductors separated by a thin type of p-type semiconductor. and p-n-p transistor is formed by two p-types separated by a thin type of n-type as shown in fig.

In each type of transistor, the following points may be noted:

- ① There are two pn junctions. (two diodes are connected back to back)
- ② There are three terminals, taken from each type of semiconductor
- ③ The middle part is a very thin layer as this is the most important factor in the function of a transistor.

Transistor As an Amplifier



A load resistor R_L is connected in series with the collector supply voltage V_{CC} of CB transistor configuration as shown in fig.

A small change in the input voltage between emitter and base, say ΔV_i , causes a relatively large change in emitter current, say ΔI_E . A fraction of this change in current is collected and passed through R_L and is denoted by symbol α . Therefore the corresponding change in voltage across the load resistor R_L due to this current is $\Delta V_o = \alpha R_L \Delta I_E$. Here, the voltage amplification $A_v = \frac{\Delta V_o}{\Delta V_i} = \frac{\alpha R_L}{R_b}$ is greater than unity and this transistor acts as an amplifier.

Emitter: It supplies charge carriers (electrons or holes) is called the emitter. The emitter is always forward biased w.r.t base so that it can supply a large number of majority carriers. The emitter is heavily doped.

~~Collector~~: It collects the charge is called the collector. The collector is always reverse biased. Its function is to remove charges from its junction with the base. The collector is moderately doped.

Base: The middle part which forms two p-n-junctions between emitter and collector is called the base. The base-emitter junction is forward biased, allowing low resistance for the emitter circuit. The base-collector junction is reverse biased and provides high resistance for the collector circuit.

The base is lightly doped. It passes most of the emitter charge carriers to the collector.

-Types of transistor amplifiers configuration

When a transistor is to be connected by a circuit, one terminal is used as an input terminal, the other terminal is used as an output terminal and the third terminal is common to the input and output. Depending upon the input, output and common terminal, a transistor amplifier can be connected by

three configurations. They are (a) common base (CB) configuration

(b) common emitter (CE) configuration, and (c) common collector (CC) configuration.

(a) CB configuration: This is also called grounded base configuration. In this configuration, emitter is the input terminal, collector is the output terminal and base is the common terminal.

(b) CE configuration: This is also called grounded emitter configuration. In this configuration, base is the input terminal, collector is the output terminal and emitter is the common terminal.

(c) CC configuration: This is also called grounded collector configuration. In this configuration, base is the input terminal, collector is the output terminal and emitter is the common terminal.

* Common Base Configuration:

The circuit diagram for determining the static characteristic curves of an NPN transistor in the common base configuration is shown in fig. ①

Input characteristics: To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volt and the emitter current I_E is increased from zero by suitable equal steps by increasing V_{EB} . This is repeated for higher fixed values of V_{CB} .

A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB} . The input characteristics thus obtained are shown in fig ②

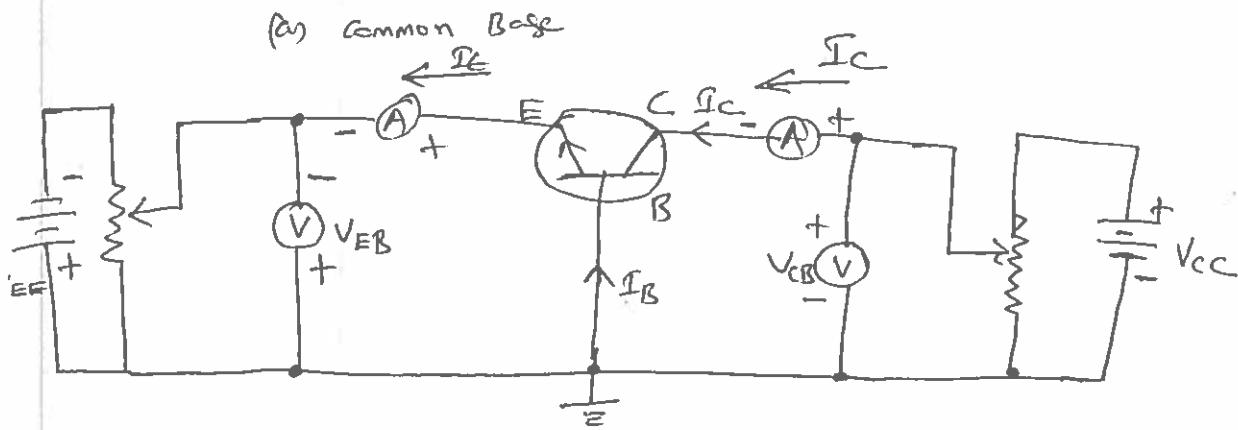
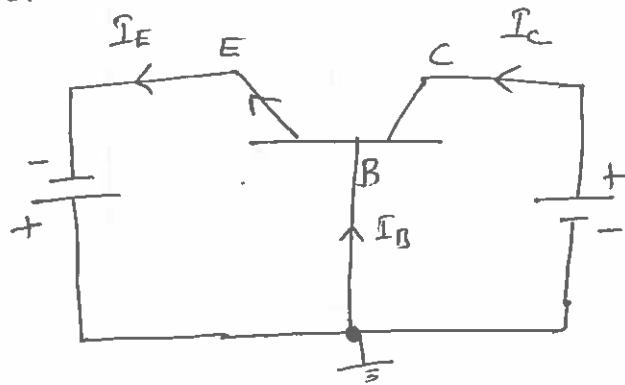


Fig ③ circuit to determine CB static characteristics.

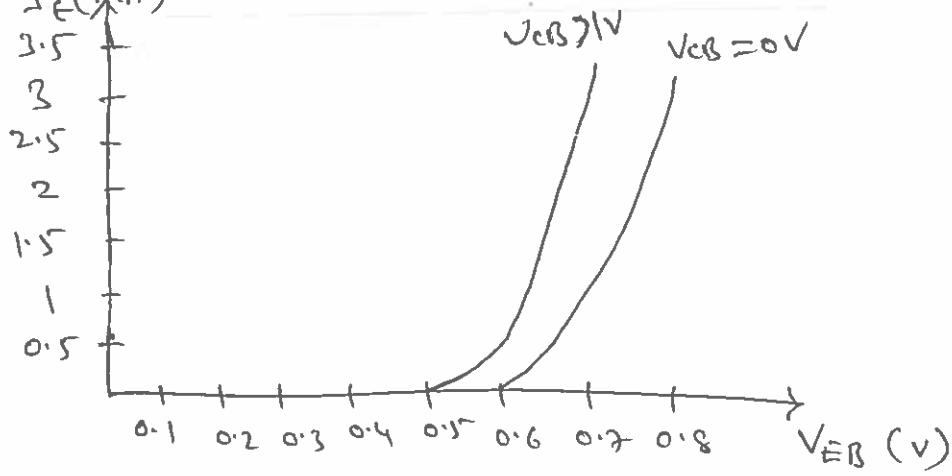


Fig: CB Input characteristics

Output characteristics:

To determine the output characteristics, the emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB} . Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of V_{CB} . This is repeated for different fixed values of I_E .

If I_E now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in fig.

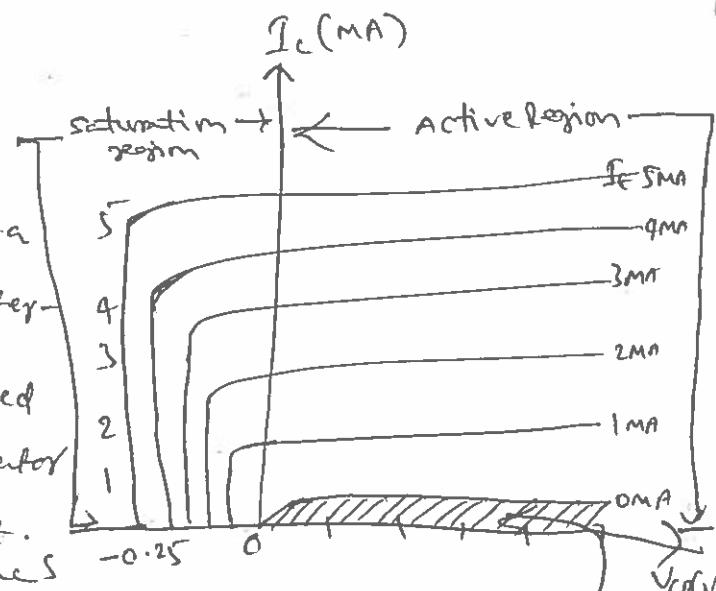


Fig: CB output characteristics
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Transistor parameters (Common Base)

The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common base hybrid parameters or h-parameters.

(a) Input Impedance (h_{ib}): It is defined as the ratio of the change in (input) emitter voltage to the change in (input) emitter current with (output) collector voltage V_{CB} kept constant. Therefore

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, V_{CB} \text{ constant.}$$

The typical value of h_{ib} ranges from 20Ω to 50Ω .

(b) Output admittance (h_{ob}): It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) emitter current I_E kept constant. Therefore

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, I_E \text{ constant.}$$

The typical value of this parameter is of the order of 0.1 to 10 μmho .

(c) Forward current gain (h_{fb}): It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant. Hence

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, V_{CB} \text{ constant.}$$

Its typical value varies from 0.9 to 1.0.

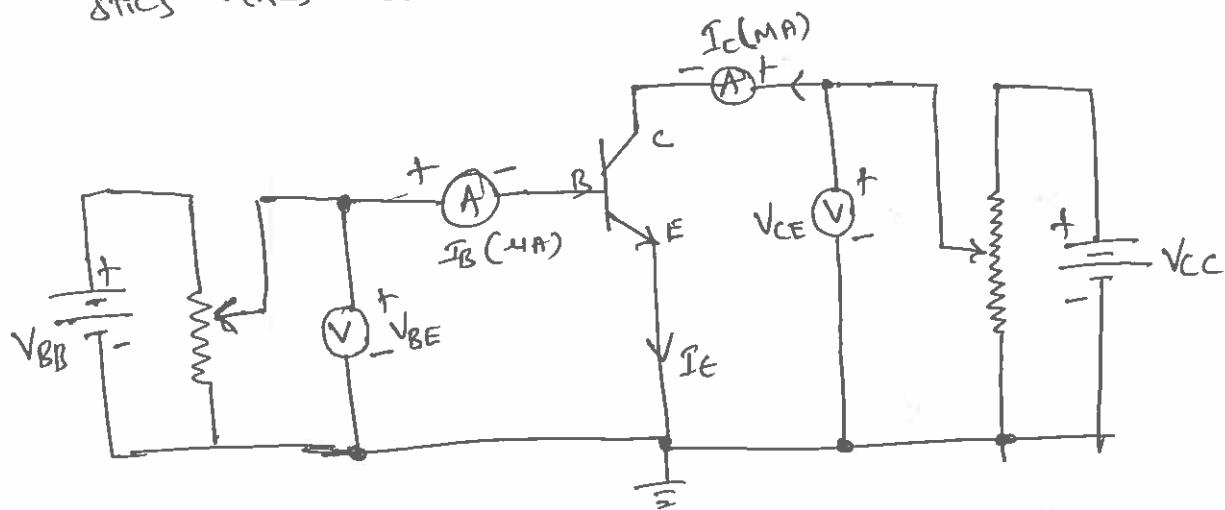
(d) Reverse voltage gain (h_{rb}): It is defined as the ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current I_E ,

$$\text{Hence } h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, I_E \text{ constant.}$$

This value is of the order of 10^{-5} to 10^4 .

Common Emitter configuration (Input and output)

Input characteristics: To determine the input characteristics, the collector to emitter voltage is kept constant at zero and base current is increased from zero in equal steps by increasing V_{BE} in the ckt shown in fig ①. The value of V_{BE} is noted for each setting of I_B . This procedure is repeated for higher fixed values of V_{CE} and the curves of $I_B \text{ vs } V_{BE}$ are drawn. The input characteristics thus obtained are shown in fig ②.



① fig: circuit to determine CE static characteristics.

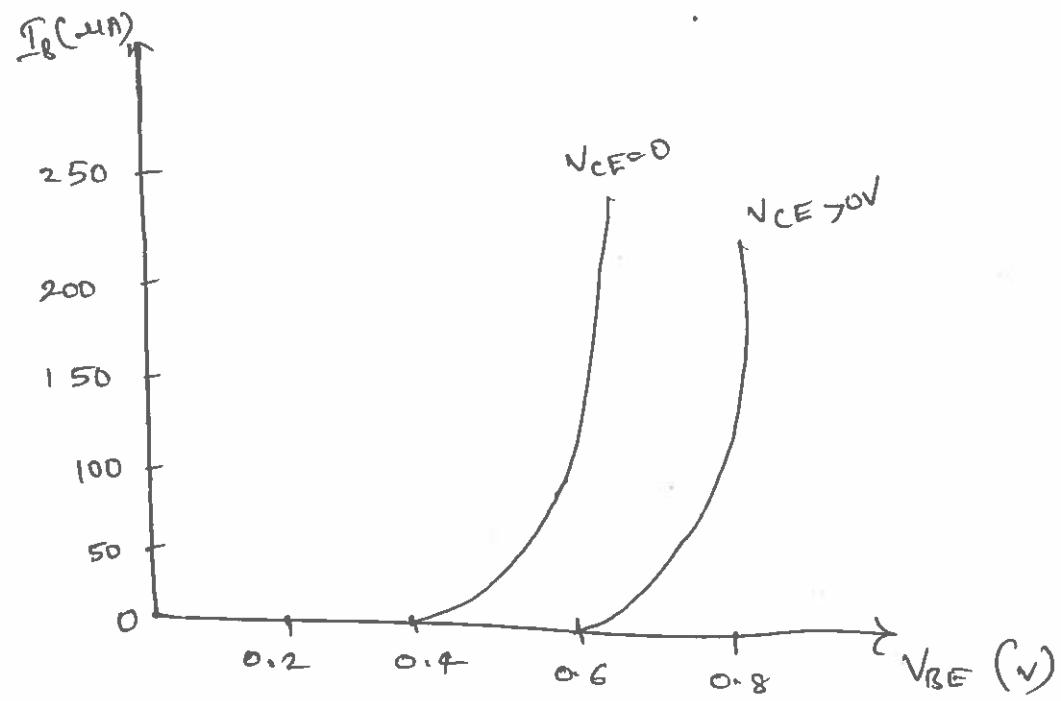
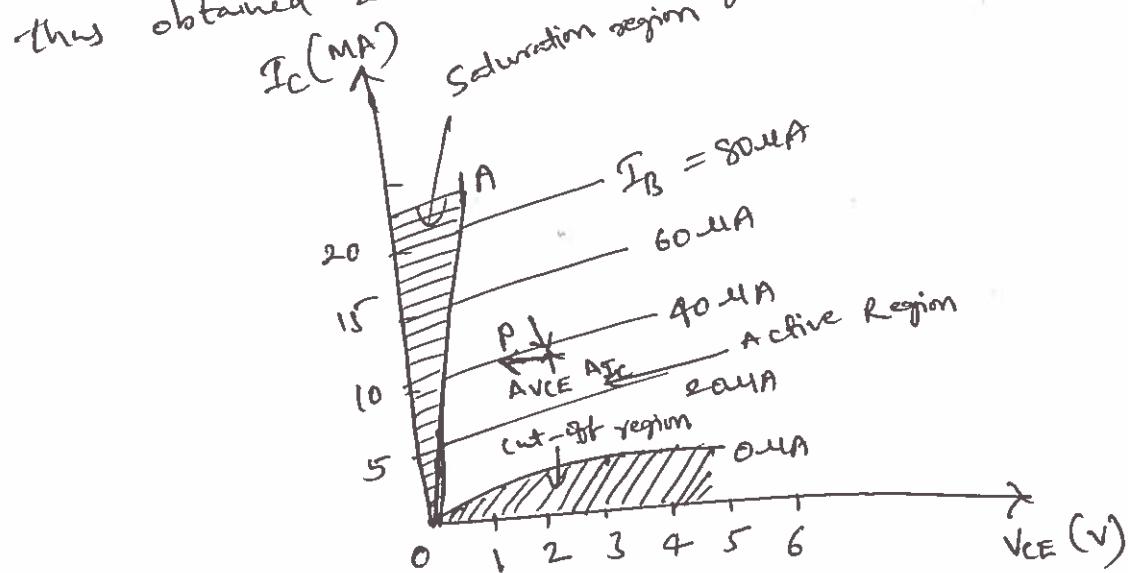


fig: CE input characteristics.

output characteristics: To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting base-emitter voltage, V_{BE} . The magnitude of collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting of V_{CE} . Now the curves of I_C versus V_{CE} are plotted for different constant values of I_B . The output characteristics thus obtained are shown in fig ③



③ fig: CE output characteristics

The output characteristics have three regions, namely, saturation region, cut-off region and active region.

Transistor parameters: The slope of the CE characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common emitter hybrid parameters or h-parameters.

(a) Input Impedance(h_{ie}): It is defined as the ratio of the change in (input) base voltage to the change in (input) base current with the (output) collector voltage V_{CE} kept constant. Therefore $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}$, V_{CE} constant

h_{ie} ranges from 500 to 2000 Ω .

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(b) output Admittance (h_{oe}): It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) base current I_B kept constant.

$$\text{Therefore, } h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, I_B \text{ constant.}$$

h_{oe} ranges from 0.1 to 10 mhos.

(c) Forward current Gain (h_{fe}): It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) base current keeping the (output) collector voltage V_{CE} constant. Hence

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, V_{CE} \text{ constant.}$$

h_{fe} varies from 20 to 200.

(d) Reverse voltage Gain (h_{re}): It is defined as the ratio of the change in the (input) base voltage and the corresponding change in (output) collector voltage with constant (input) base current, I_B . Hence

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, I_B \text{ constant}$$

This value is of the order of 10^5 to 10^9 .

Common collector configuration:

The circuit diagram for determining the static characteristics of an NPN transistor in the common collector configuration is shown in fig.

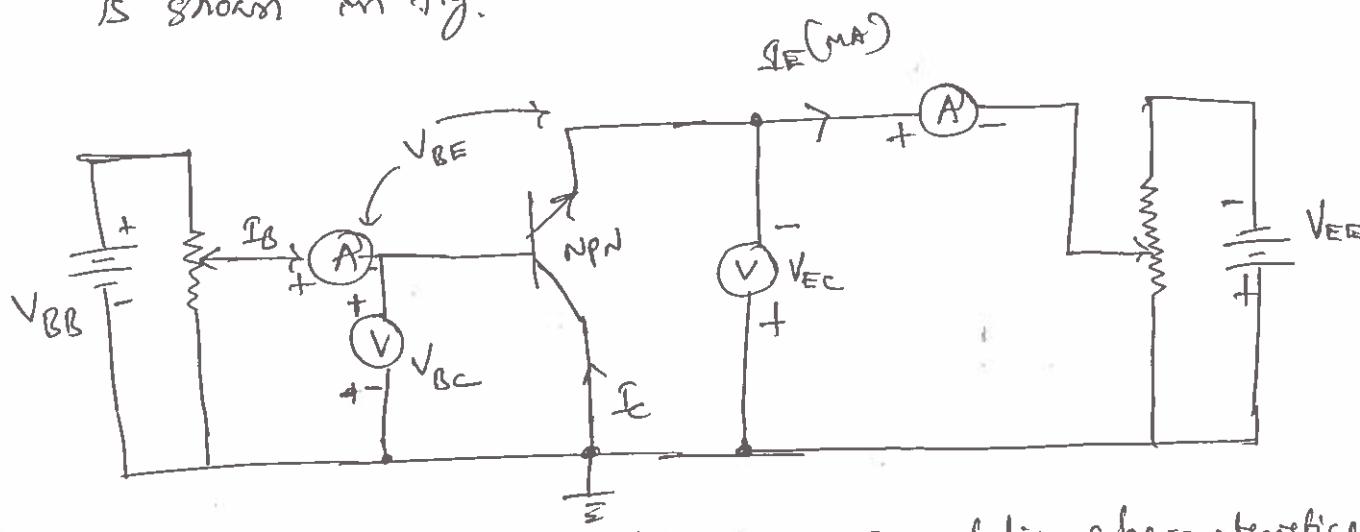


fig: circuit to determine cc static characteristics.

Input characteristics: To determine the input characteristics, V_{EC} is kept at a suitable fixed value. The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC} . Plots of V_{BC} versus I_B for different values of V_{EC} shown in fig. These are the input characteristics.

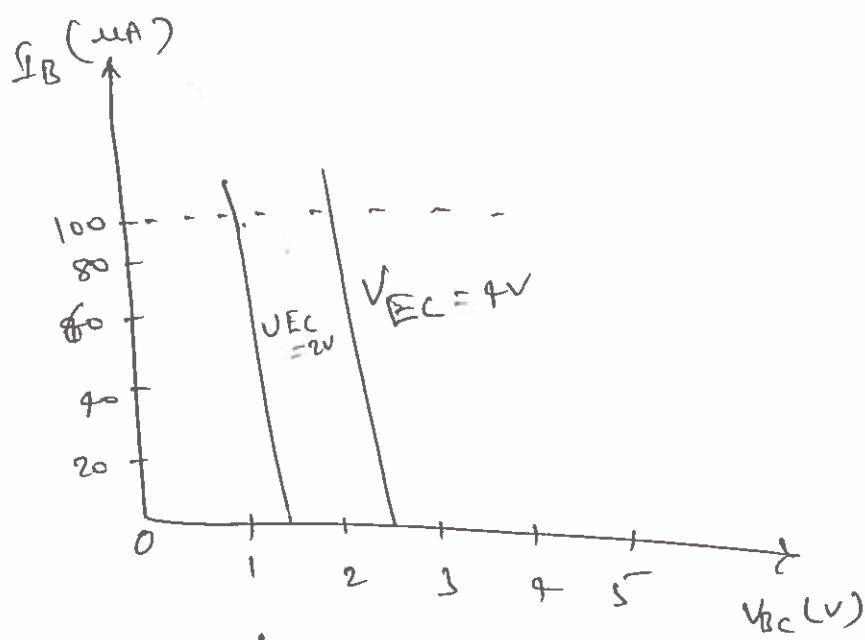


fig: cc input characteristics

Output characteristics:

The output characteristics shown in fig. are the same \rightarrow those of the common emitter configuration.

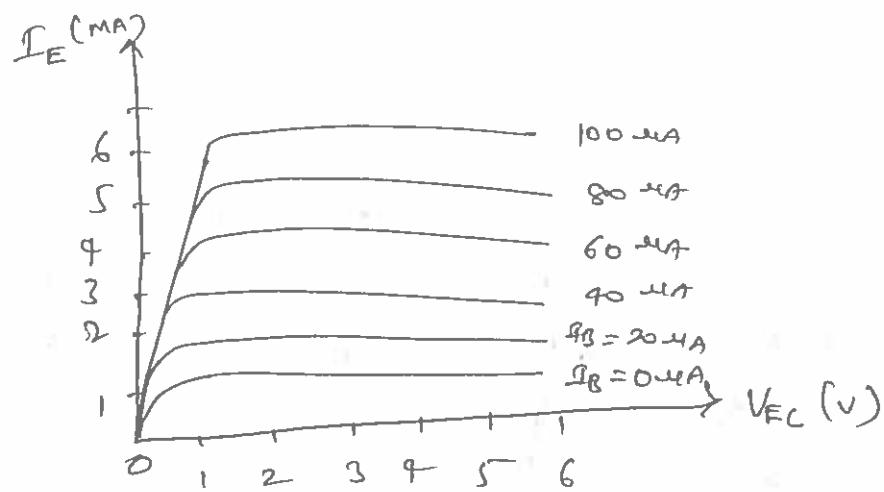


Fig: CC output characteristics.

Comparison of CB, CE and CC configurations.

Property	CB	CE	CC
Input resistance	Low (about 100 Ω)	moderate (about 750 Ω)	High (about 750k Ω)
Output resistance	High (about 450k Ω)	moderate (about 45k Ω)	low (about 25k Ω)
Current gain	1	High	High
Voltage gain	about 150	About 500	less than 1
Phase shift between input & output voltages	0 or 360°	180°	0 or 360°
Applications	For high frequency circuit	For radio frequency circuit	For impedance matching

Relation among α, β and γ

In the CC transistor amplifier circuit, I_B is the input current and I_C is the output current

$$\therefore \gamma = \frac{\Delta I_E}{\Delta I_B}$$

Substituting $\Delta I_B = \Delta I_E - \Delta I_C$

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator on RHS by ΔI_E , we get

$$\frac{\gamma = \frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E - \Delta I_E}{\Delta I_E}} = \frac{1}{1-\alpha}$$

$$\therefore \gamma = \frac{1}{1-\alpha} = (\beta + 1)$$

=====

Transistor Parameters:

Current amplification factor:

In a transistor amplifier with ac input signal, the ratio of change in output current to the change in input current is known as the current amplification factor.

In the CB configuration the current amplification factor,

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

In the CE configuration the current amplification factor,

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

In the CC configuration the current amplification factor,

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Relationship between α and β :

We know that $\Delta I_E = \Delta I_C + \Delta I_B$

By definition, $\Delta I_C = \alpha \Delta I_E$

$$\therefore \Delta I_E = \alpha \Delta I_E + \Delta I_B$$

$$\Delta I_B = \Delta I_E - \alpha \Delta I_E$$

$$\Delta I_B = \Delta I_E (1 - \alpha)$$

Dividing both sides by ΔI_C , we get

$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E (1 - \alpha)}{\Delta I_E} (1 - \alpha)$$

$$\therefore \frac{1}{\beta} = \frac{1}{\alpha} (1 - \alpha)$$

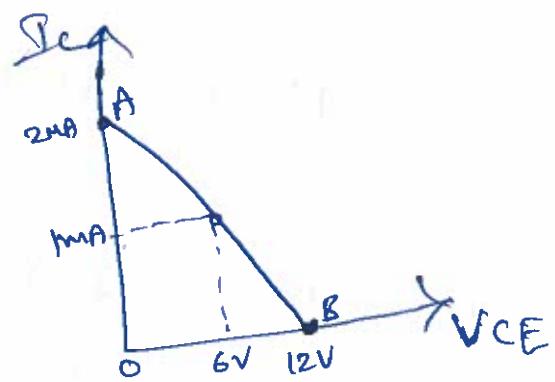
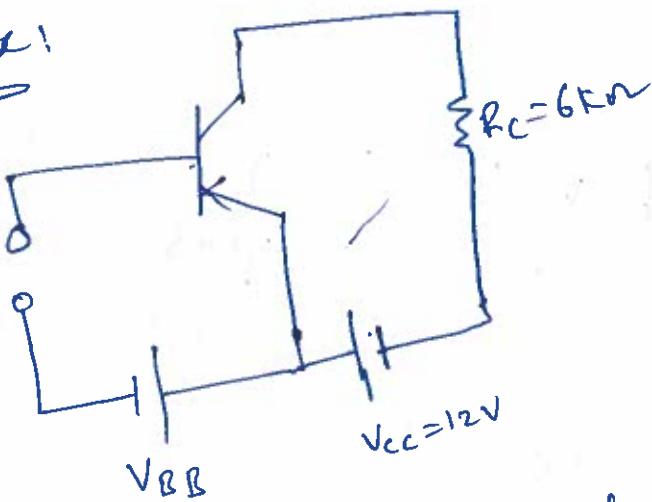
$$\beta = \frac{\alpha}{(1 - \alpha)} \quad \left(\begin{array}{l} \alpha(1 - \alpha) = \alpha \\ \beta - \beta\alpha = \alpha \end{array} \right)$$

Rearranging, we also get $\alpha = \frac{\beta}{1 + \beta}$, or $\frac{1}{\alpha} - \frac{1}{\beta} = 1$

The operating point!

The zero signal values of I_C and V_{CE} of transistor is known as operating point. It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied. It is also called α quiescent (silent) point or α -point.

Ex:



In the above circuit diagram if $V_{CC} = 12V$ and $R_C = 6k\Omega$, draw the d.c load line. What will be the α point if zero signal base current is 2mA ($\beta = 50$)?

The collector-emitter voltage V_{CE} is given by

$$V_{CE} = V_{CC} - I_C R_C$$

when $I_C = 0$, $V_{CE} = V_{CC} = 12V$. This locates the point B of the load line.

when $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C} = \frac{12}{6k\Omega} = 2mA$. This locates the point A of the load line.

By joining these two points, load line OP is constructed as shown in fig ②

i) zero signal base current, $I_B = 20 \mu A = 0.02mA$

current amplification factor $B = 50$

\therefore zero signal collector current

$$I_C = BI_B = 50 \times 0.02 = 1mA$$

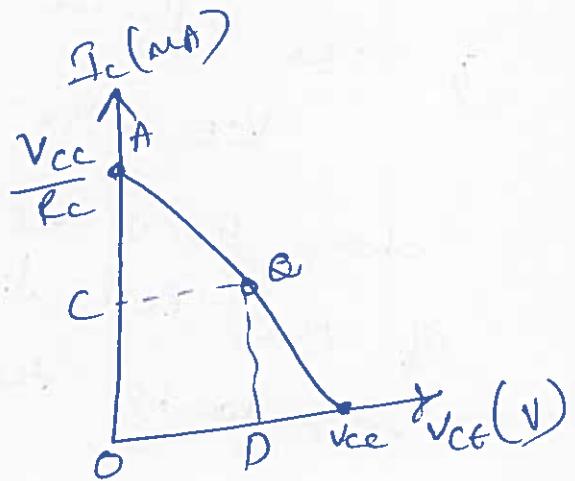
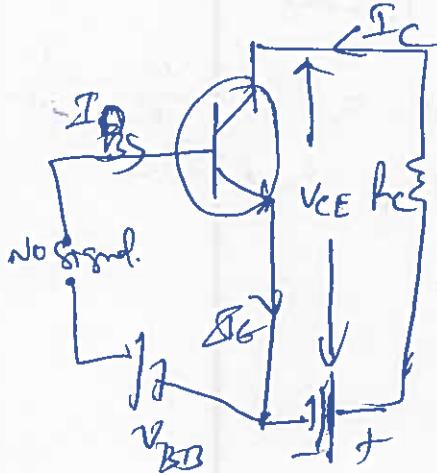
zero signal collector-emitter voltage

$$V_{CE} = V_{CC} - I_C R_C = 12 - 1mA \times 6k\Omega = 6V$$

operating point is 6V, 1mA.

The current (I_C) and voltage (V_{CE}) conditions for the transistor circuit are represented by some point on the output characteristics. The same information can be obtained from the load line. When I_C is maximum ($= \frac{V_{CC}}{R_C}$), then $V_{CE} = 0$. If $I_C = 0$, then V_{CE} is maximum and is equal to V_{CC} . For any other value of collector current say O_C , the collector-emitter

voltage $V_{CE} = O_D$.



factors effecting the Q-point

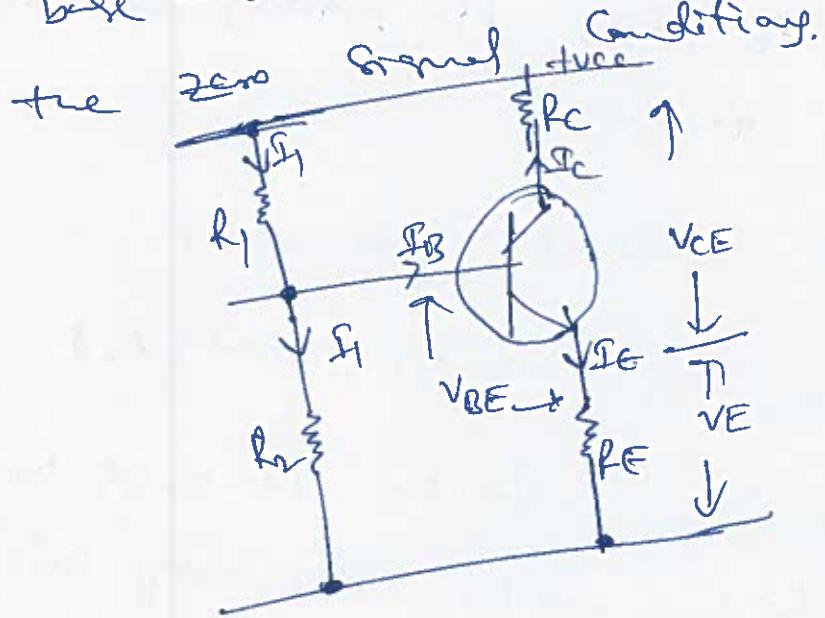
once the operating point is fixed, it is expected to be stable. But the operating point (Q -point) tends to shift its position due to the following factors.

- ① Variations in transistor parameter
- ② Any changes in collector current (I_C)
- ③ changes in the collector leakage current (I_{CEO}) which doubles for every $10^\circ C$ increase in temperature
- ④ change in temperature

→ self bias (or) emitter bias (or) voltage divider bias

This is the most widely used method of providing biasing and stabilization to a transistor. In this method, two resistances R_1 and R_2 are connected across the supply voltage V_{CC} and provide biasing. The emitter ~~bias~~ resistance (R_2) provides stabilization. The name "voltage divider" comes from the voltage divider formed by R_1 and R_2 .

The voltage drop across R_2 forward biases the base-emitter junction. They cause the base current and hence collector current flowing through the zero signal source.



Circuit analysis

Suppose that the current flowing through resistance R_1 is I_1 . As base current I_B is very small, therefore, it can be assumed with reasonable accuracy that current flowing through R_2 is also I_1 .

∴ Collector current I_C :

$$I_C = \frac{V_{CC}}{R_1 + R_2}$$

i. voltage across resistance R_2

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2} \right) R_2$$

i. voltage across resistance R_1 .

$$V_1 = \left(\frac{V_{CC}}{R_1 + R_2} \right) R_1$$

Applying Kirchhoff's voltage law to the base circuit

Biasing

The process of giving proper supply voltages and resistances for obtaining the desired Q-point is called biasing.

The collector current for common-emitter amplifier is expressed by,

$$I_c = R_B + I_{CEO}$$

Types of Biasing Circuits

- (1) fixed bias (or) base resistor bias
- (2) collector-to-base (or) biasing with collector feed back resistor.
- (3) potential divider bias (or) self bias
- (or) voltage divider bias (or) universal bias

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Unit-2Transistor Biasing and Stabilization

Transistor Biasing: The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as Transistor Biasing.

Stabilisation: The process of making operating point independent of temperature changes or variations in transistor parameters is known as stabilization.

Transistor Biasing:

The basic function of Transistor is to do amplification. The weak signal is given to the base of the transistor and amplified output is obtained in the collector circuit. One important requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. The process of raising the strength of a weak signal without any change in its general shape is known as faithful amplification.

The theory of Transistor reveals that it will function properly if its input circuit (i.e. base-emitter junction) remains forward biased and output circuit (i.e. collector-base junction) remains reverse biased at all times. This is then the key factor for getting faithful amplification. To ensure this the following basic conditions must be satisfied.

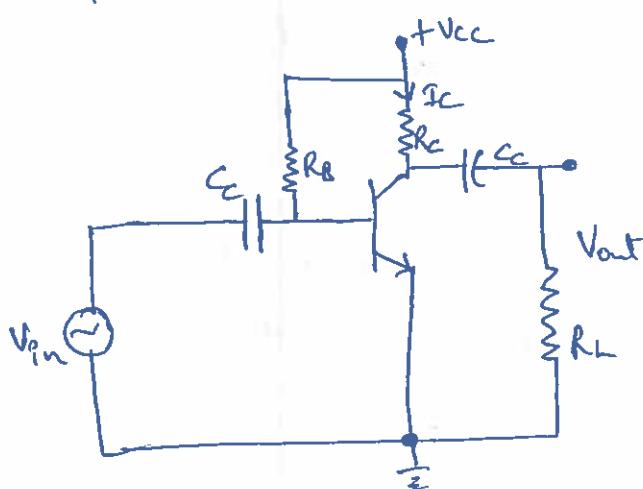
- ① proper zero signal collector current
 - (2) minimum proper base-emitter voltage at any instant
 - (3) minimum proper collector-emitter voltage (V_{CE}) at any instant.
- * The process of giving proper supply voltage and resistances for obtaining the desired Q-point is called biasing.

The collector current for common-emitter amplifier is expressed by.

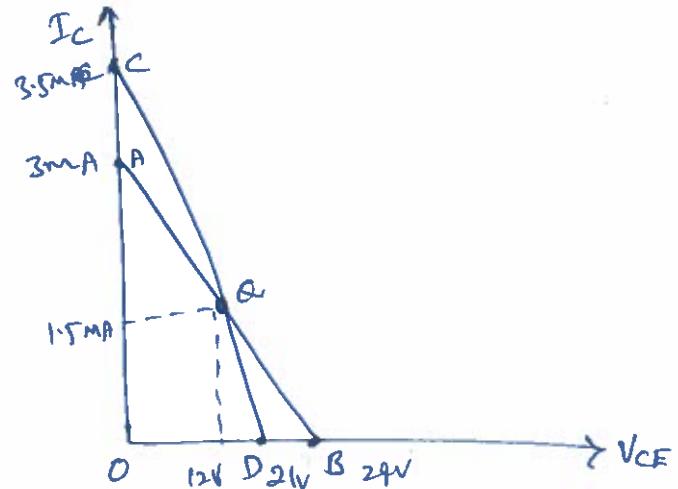
$$I_C = \beta I_B + I_{CEO} = (1 + \beta) I_{CO}$$

=

DC load line:



(a)



(b)

fig: (a) Biasing circuit (b) CE output characteristics and load line

In fig (a) the values of V_{CC} and R_C are fixed and I_C and V_{CE} are dependent on R_B .

Applying KVL to the collector circuit for (a), we get

$$V_{CC} = I_C R_C + V_{CE}$$

The straight line represented by AB in fig(b) is called the dc load line. The coordinates of the end point A are obtained by substituting $V_{CE} = 0$ and in the above equation. Then $I_C = \frac{V_{CC}}{R_C}$.

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(2)

The coordinates of A are $V_{CE}=0$ and $I_C = \frac{V_{CC}}{R_L}$.

The coordinates of B are obtained by substituting $I_C=0$ for the above equation. Then $V_{CE} = V_{CC}$. Therefore the coordinates of B are $V_{CE}=V_{CC}$ and $I_C=0$. The dc load line AB can be drawn if the values of R_L and V_{CC} are known.

As shown in fig(b), the optimum Q-point is located at the midpoint of the dc load line AB between the saturation and cutoff regions. i.e. Q is exactly midway between A and B. In order to get faithful amplification, the Q-point must be well within the active region of the transistor.

④ AC load lines

After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is selected under zero input signal condition of the circuit. Here, the ac load line should also pass through the operating point Q. The effective ac load resistance, R_{AC} , is the combination of R_L parallel to R_L , i.e. $R_{AC} = R_L // R_L$. So the slope of the ac load line CD will be ($\pm \frac{1}{R_{AC}}$).

To draw an ac load line, two end points, maximum V_{CE} and maximum I_C when the signal is applied are required.

Maximum $V_{CE} = V_{CEQ} + I_{CQ} \cdot R_{AC}$, it locates the point D(0) on the V_{CE} axis.

Maximum $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{AC}}$, it locates the point C(0) on the I_C axis.

By joining points C and D, an ac load line CD is constructed. As $R_C > R_{AC}$, the dc load line is less steep than the ac load line.

* Fixed Bias or Base Resistor method

A common emitter amplifier using fixed bias circuit is shown in fig. The dc analysis of the circuit yields the following equation.

$$V_{CC} = I_B R_B + V_{BE}$$

Therefore $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

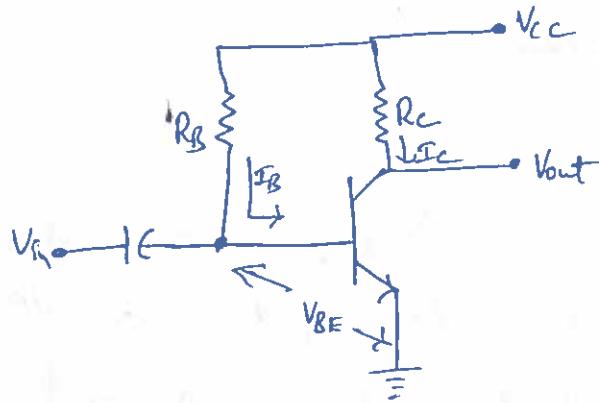


fig: Fixed Bias.

Since this equation is independent of current I_C , $\frac{d\alpha}{dI_C} = 0$ and the stability factor given in eqn. ($S = \frac{1+\beta}{1-\beta \left(\frac{d\beta}{dI_C} \right)}$) reduces to $S = 1+\beta$.

Since β is a large value quantity, this is a very poor bias stable circuit. Therefore, in practice, this circuit is not used for biasing the base.

The advantage of this method are

- (a) Simplicity (b) Small number of components required.

(\square)

(5)

→ Emitter - Feedback Bias

The emitter-feedback bias network shown in fig. contains an emitter resistor for improving the stability level over that of the fixed-bias configuration. The analysis will be performed by first examining the base-emitter loop and then using the results to investigate the collector-emitter loop.

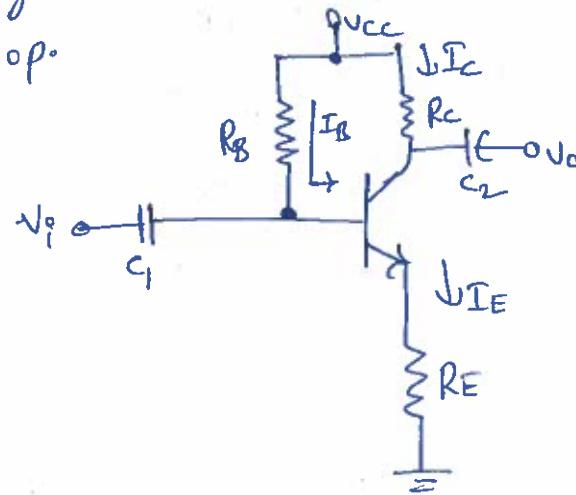


fig : Emitter-feedback Bias circuit.

Base-Emitter Loops Applying KVL for the base-emitter loop, we get

$$V_c - I_B R_B - V_{BE} - I_E R_E = 0 \quad \text{--- (1)}$$

$$V_{cc} - I_B R_B - V_{BE} - (I_B + I_c) R_E = 0$$

$$V_{cc} - I_B (R_B + R_E) - V_{BE} - I_c R_E = 0$$

$$V_{cc} - V_{BE} = I_B (R_B + R_E) + I_c R_E$$

Therefore $I_B = \frac{V_c - V_{BE}}{R_E + R_B} - \left(\frac{R_E}{R_E + R_B} \right) I_c \quad \text{--- (2)}$

Here V_{BE} is independent of I_c

Hence $\frac{dI_B}{dI_c} = - \left(\frac{R_E}{R_E + R_B} \right) \quad \text{--- (3)}$

$$\text{substituting eqn (3) in } S = \frac{1+\beta}{1-\beta \left(\frac{dI_B}{dI_C} \right)}$$

$$S = \frac{1+\beta}{1+\beta \frac{R_E}{R_E+R_B}} \quad \text{--- (4)}$$

Since $1 + \frac{\beta R_E}{(R_E + R_B)} > 1$, $S < (1+\beta)$. note that the value of the stability factor S is always lower in emitter- feedback bias circuit than that of the fixed bias circuit.

Collector - Emitter loop

Applying KVL for the collector - emitter loop we get.

$$I_E R_E + V_{CE} + I_{C_E} - V_C = 0$$

Substituting $I_E = I_C$ we have

$$V_{CE} - V_C + I_C (R_C + R_E) = 0$$

$$\text{and } V_{CE} = V_C - I_C (R_C + R_E)$$

V_E is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E$$

The voltage from collector to ground ~~then~~ can be determined from

$$V_{CE} = V_C - V_E$$

$$\text{and } V_C = V_E + V_C$$

$$(or) V_C = V_C - I_C R_C$$

The voltage at the base with respect to ground can be determined from

$$V_B = V_C - I_B R_E \quad (or) \quad V_B = V_{BE} + V_E$$

(P)

Collector - Feedback Bias (or) collector-to-base bias

If the collector current I_C tends to increase due to either increase in temperature or the transistor has been replaced by the one with a higher β , the voltage drop across R_C increases, thereby reducing the value of V_{CE} . Therefore, I_B decreases, ^{which} in turn, compensates the increase in I_C . Thus greater stability is obtained.

The loop equation for this circuit is

$$V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE} \quad \text{--- (1)}$$

$$\text{i.e } I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \quad \text{--- (2)}$$

$$\text{Therefore } \frac{dI_B}{dI_C} = \frac{R_C}{R_C + R_B} \quad \text{--- (3)}$$

substituting eq. in

$$S = \frac{1+\beta}{1-\beta} \left(\frac{dI_B}{dI_C} \right)$$

we get

$$S = \frac{1+\beta}{1+\beta \left(\frac{R_C}{R_C + R_B} \right)} \quad \text{--- (P)}$$

This value of the stability factor is smaller than the value obtained by fixed bias circuit. Also, S can be made small and the stability can be improved by making R_B small or R_C large.

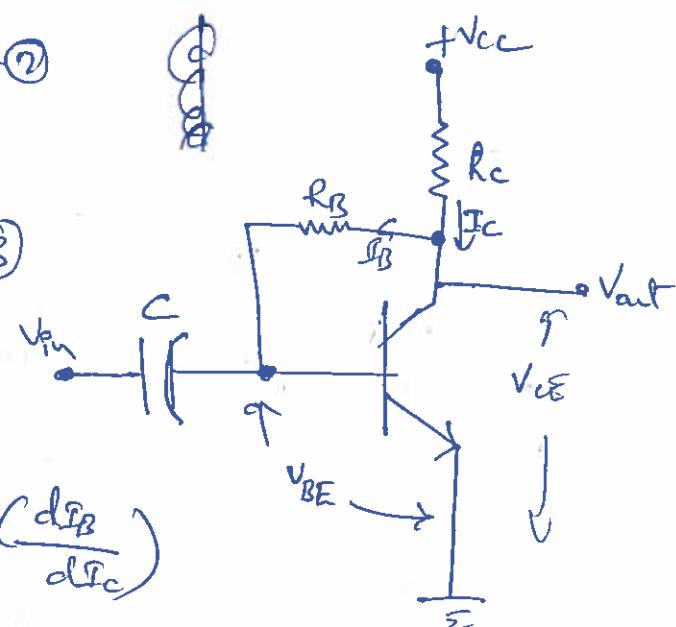


fig: collector-to-base
Bias circuit

if R_C is very small, then $\beta = \beta + 1$, i.e. stability is very poor. Hence, the value of R_C must be quite large for good stabilization.

Collector-Emitter feedback bias:

Fig shows the collector-emitter feedback bias circuit that can be obtained by applying both the collector-feedback and emitter-feedback. Here collector-feedback is provided by connecting a resistance R_B from the collector to the base and emitter-feedback is provided by connecting an emitter resistance R_E from the emitter to ground. Both the feedbacks are used to control the collector current I_C and the base current I_B in the opposite direction to increase the stability of compared to the previous biasing circuits.

Applying KVL to the current we get:

$$(I_B + I_C)R_E + V_{BE} + I_B R_B + (I_B + I_C)R_C - V_C = 0$$

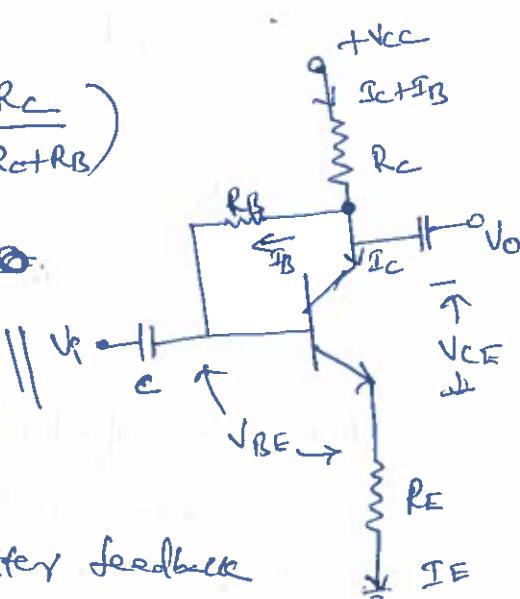
$$\text{Therefore, } I_B = \frac{V_C - V_{BE}}{R_E + R_C + R_B} - \left(\frac{R_E + R_C}{R_E + R_C + R_B} \right) I_C$$

Since V_{BE} is independent of I_C ,

$$\frac{dI_B}{dI_C} = - \left(\frac{R_E + R_C}{R_E + R_C + R_B} \right)$$

Substituting the above equation in S :

$$S = \frac{1 + \beta}{1 + \beta (R_E + R_C)} \parallel \frac{V_C}{R_E + R_C + R_B}$$

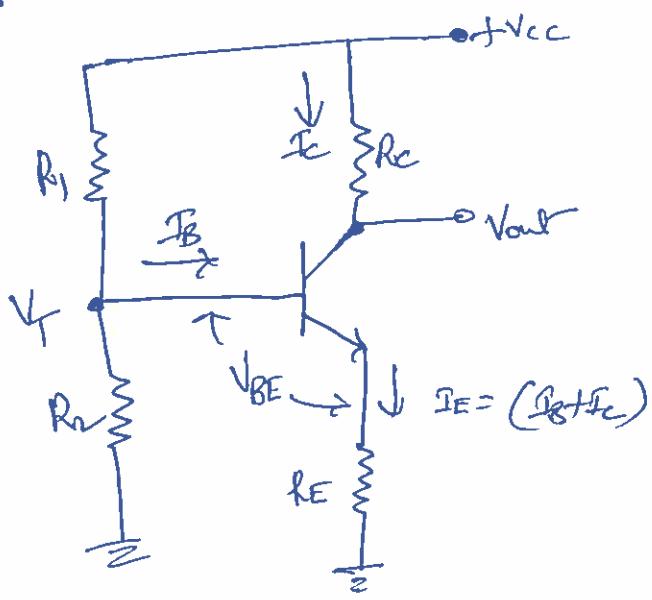


- The stability of the collector-emitter feedback bias circuit is always better than that of the collector-feedback and emitter-feedback circuits.

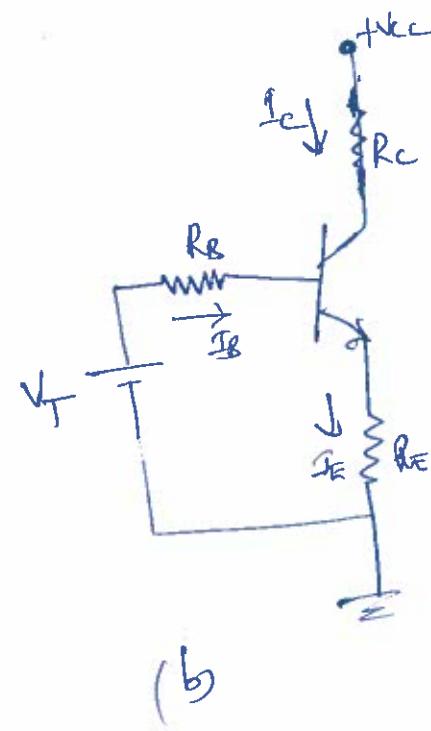
(5)

* Voltage Divider Bias, Self Bias, or Emitter Bias

The self bias, also called as emitter bias, or emitter resistor and potential divider circuit, that can be used for low collector resistance, is shown by fig. The current in the emitter resistor R_E causes a voltage drop which is in the direction to reverse bias the emitter junction. For the transistor to remain in the active region, the base-emitter junction has to be forward biased. The required base bias is obtained from the power supply through the potential divider network of the resistors R_1 and R_2 .



(a)



(b)

Fig: (a) self Bias (b) Thevenin's Equivalent Circuit

* Use of self-Bias Circuit as a Constant Current Circuit

Ques. 1. Explain the following terms with suitable examples.

a) Open circuit voltage & short circuit current.

b) Series and shunt resistances & parallel resistances.

c) Induced EMF & Induced current & Induced voltage.

d) Induced EMF & Induced current & Induced voltage.

e) Induced EMF & Induced current & Induced voltage.

f) Induced EMF & Induced current & Induced voltage.

g) Induced EMF & Induced current & Induced voltage.

h) Induced EMF & Induced current & Induced voltage.

i) Induced EMF & Induced current & Induced voltage.

j) Induced EMF & Induced current & Induced voltage.

k) Induced EMF & Induced current & Induced voltage.

l) Induced EMF & Induced current & Induced voltage.

m) Induced EMF & Induced current & Induced voltage.

n) Induced EMF & Induced current & Induced voltage.

o) Induced EMF & Induced current & Induced voltage.

p) Induced EMF & Induced current & Induced voltage.

q) Induced EMF & Induced current & Induced voltage.

r) Induced EMF & Induced current & Induced voltage.

s) Induced EMF & Induced current & Induced voltage.

t) Induced EMF & Induced current & Induced voltage.

u) Induced EMF & Induced current & Induced voltage.

v) Induced EMF & Induced current & Induced voltage.

w) Induced EMF & Induced current & Induced voltage.

x) Induced EMF & Induced current & Induced voltage.

y) Induced EMF & Induced current & Induced voltage.

z) Induced EMF & Induced current & Induced voltage.

aa) Induced EMF & Induced current & Induced voltage.

bb) Induced EMF & Induced current & Induced voltage.

cc) Induced EMF & Induced current & Induced voltage.

dd) Induced EMF & Induced current & Induced voltage.

QUESTION AND ANSWER

The various biasing circuits considered in the previous sections used some types of negative feedback to stabilise the operation point. Diodes, thermistors and transistors can be used to compensate for variations in current.

Diode Compensation:

fig shows a transistor amplifier with a diode D connected across the base-emitter junction for compensation of change in collector saturation current I_{CO} .

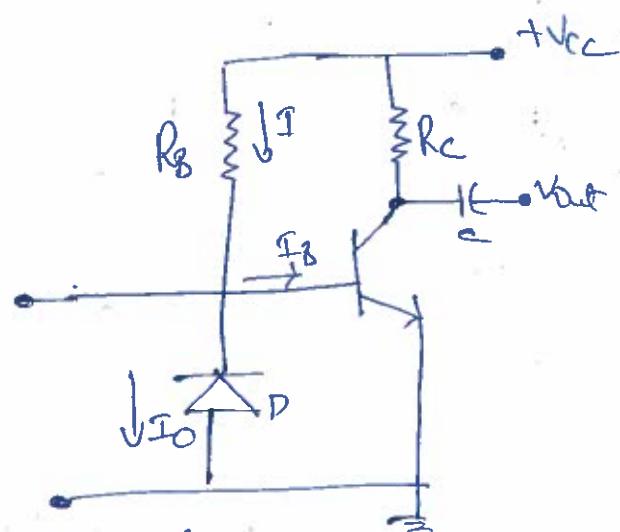


fig: Diode Bias Compensation.

$$\text{The Base current } I_B = I - I_0$$

As long as temperature is constant, diode D operates as a resistor. As the temperature increases, I_{CO} of the transistor increases. Hence, to compensate for this, the base current I_B should be decreased.

The increase in temperature will also cause the leakage current I_0 through D to increase and thereby decreasing the base current I_B . This is the required action to keep I_B constant.

Thermistor Compensation:

In a fig. thermistor, R_T , having a negative temperature coefficient is connected in parallel with R_E . The resistance of thermistor decreases exponentially with increase of temperature. An increase in temperature will decrease the base voltage V_{RE} , reducing I_B and I_C . Bias stabilization is also provided by R_E and R_C .

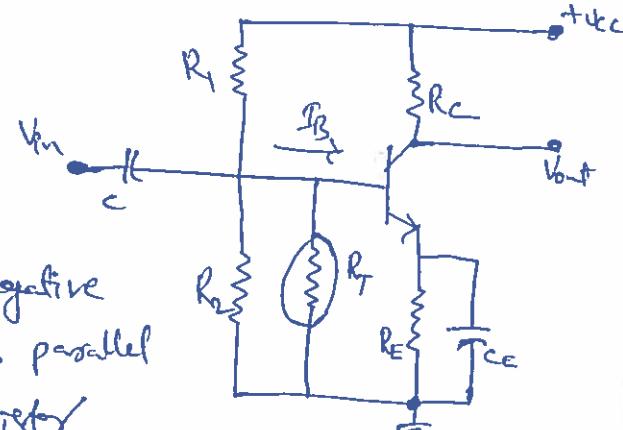


fig: Thermistor Bias compensation.

Sensistor Compensation

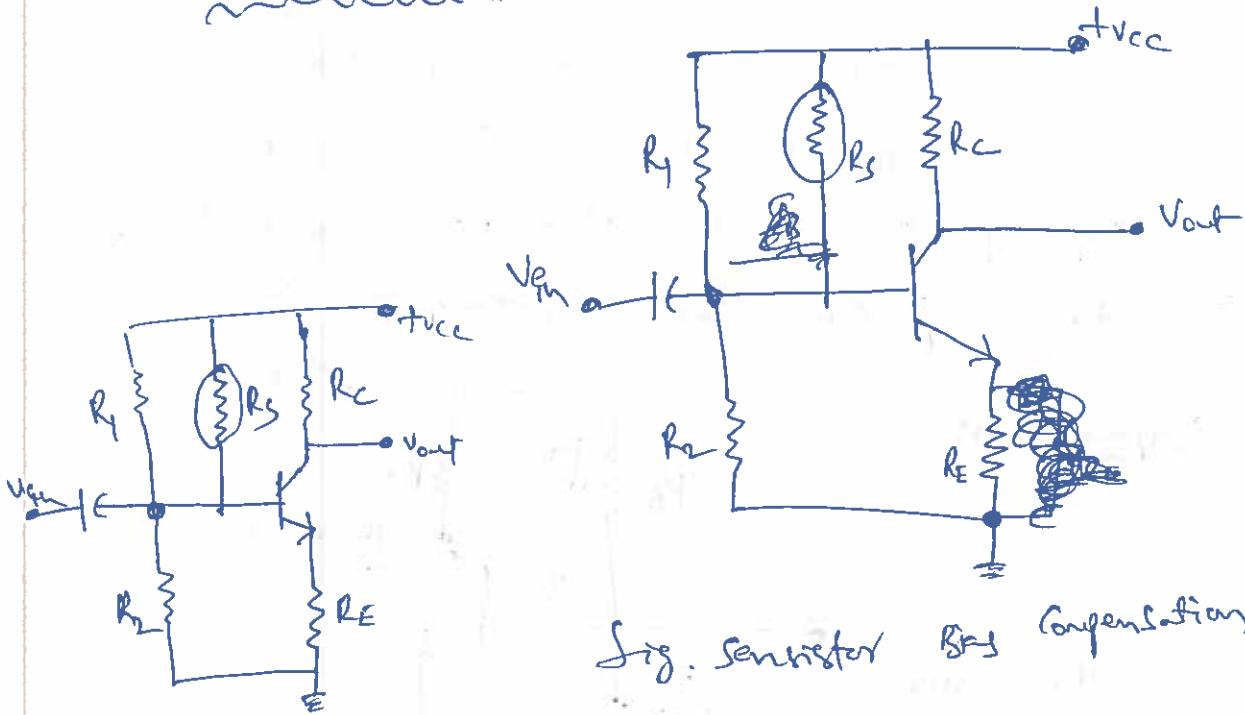


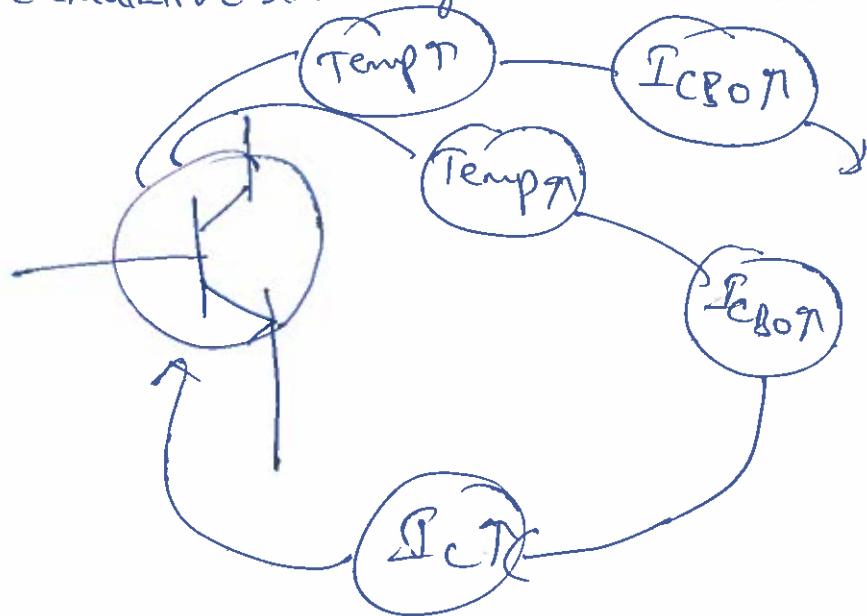
Fig. Sensistor Bias Compensation

In a fig. a sensistor, R_s , having a positive temperature coefficient is connected across R_1 (or R_E). R_s increases with temperature. As temperature increases, the equivalent resistance of the parallel combination of R_1 and R_s also increases and hence the base voltage V_{BE} decreases reducing I_B and I_C . This reduced I_C compensates for the increased I_C caused by the increase in I_{CO} , V_{BE} and β due to temperature rise.

The collector current for the CE circuit is given by

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

The three variables in the equation, β , I_B and I_{CBO} increase with rise in temperature. In particular, the reverse saturation current or leakage current I_{CBO} changes greatly with temperature. It doubles for every 10°C rise in temperature. The collector current I_C causes the collector-base junction temperature to rise. In turn, increase I_{CBO} , as a result I_C will increase still further. This process will become cumulative leading to "thermal runaway".



The collector current for a CE amplifier is given by

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

④ Stability (or) stability factor: Transistor parameter (β and V_{BE}) is ~~fixed~~ ^{constant}.

stabilization: The process of making operating point independent of temperature changes (or) variations in the rate of change of collector current I_C .

w.r.t. the collector leakage current I_{CO} at constant β and I_B is called stability factor.

$$\text{stability factor } S = \frac{dI_C}{dI_{CO}}$$

The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO} .

The general expression of stability factor for a C-E configuration can be obtained

$$I_C = \beta I_B + I_{CO}$$

Differentiating above expression w.r.t. I_C , we get

$$I_C = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

$$I_C = \beta \frac{dI_B}{dI_C} + (\beta + 1) S$$

$$S = \frac{\beta + 1}{1 - \beta \left(\frac{dI_B}{dI_C} \right)}$$

$$\left[\therefore \frac{dI_{CO}}{dI_C} = \frac{1}{S} \right]$$

The following are the factors that effect the stability of the operating point.

1) Temperature dependence of I_C

2) Change of V_{BE} and β due to replace one transistor

3) Thermal runaway.

$$V_2 = V_{BG} + V_E$$

$$V_L = V_{BF} + I_{left} R_E$$

$$(00) \quad I_E = \frac{V_L - V_{BE}}{R_E}$$

Since $I_E \approx I_C$

$$I_C = \frac{V_2 - V_{BE}}{R_E}$$

I_c does not depend on B .

(ii') collector - emitter voltage V_{CE} .
 applied Kirchhoff's voltage law to find
 collector base node

$$V_{CC} = I_{CBE} + V_{CE} + I_{CE} R_E$$

$$= I_{CBE} + V_{CE} + I_{SBE}$$

$$= T_c (R_{ct} + R_{t\ell}) + V_{CE}$$

$$V_{CF} = V_{CC} - I_C(R_C + R_F)$$

Stabilization

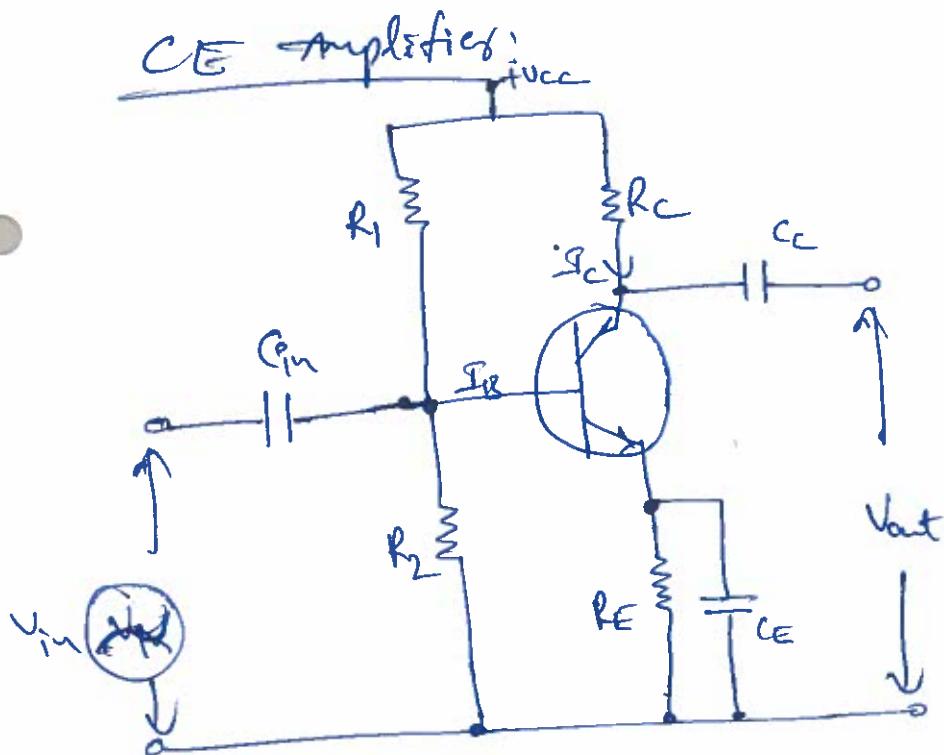
$$V_{2-} = V_B \epsilon + I_C R_E$$

excellent stabilization is provided by P.S.

Stability factor = 1

①

Amplifier: Amplifier is defined as an electronic circuit which increases the voltage, current and power of the signal.



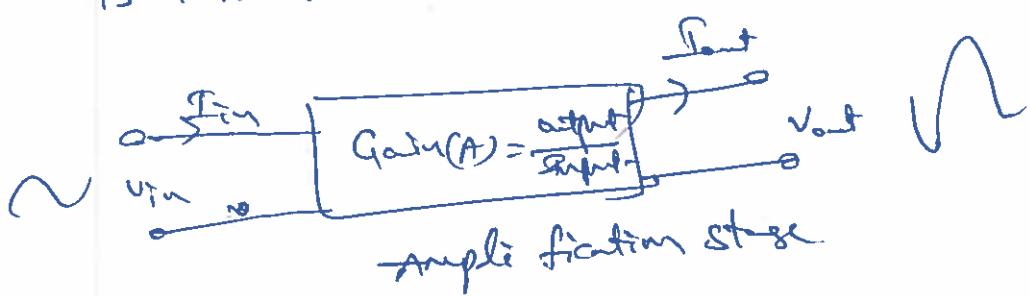
1) Biassing circuit: The resistors R_1 and R_2 forming the biassing and R_E is stabilization circuit. It sets the proper operating point for the amplifier.

2) Input capacitor (C_{in}): This capacitor C_{in} is used to couple the input signal to the base of the transistor. It blocks any D.C components present in the signal and allows only A.C signal for amplification.

② Emitter Bypass Capacitor: C_E : An emitter bypass capacitor C_E is connected to parallel with R_E to provide a low reactance path to the amplified A.C signal. If it is not used, then amplified A.C signal flowing through R_E will cause a voltage drop across it, reducing the output voltage.

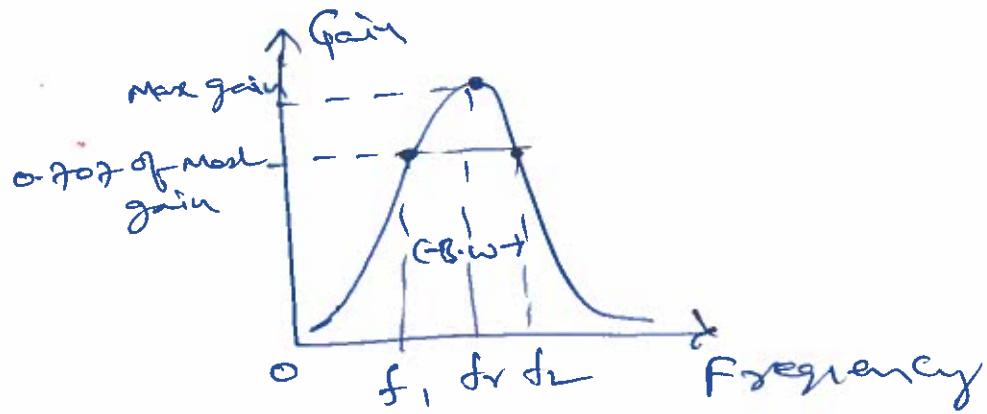
③ Coupling Capacitor C_C : The coupling capacitor C_C couples (connect) one stage of amplifier to the next stage. It blocks D.C signal and allows only A.C part of the amplified signal.

Gain: The ratio of the output electrical quantity to the input electrical quantity is known as gain.



Bandwidth: The range of frequency over which the gain is equal to or greater than 70.7% of maximum gain is known as Bandwidth.

(2)



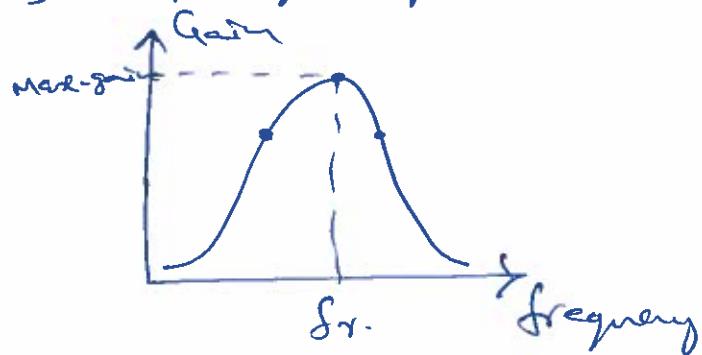
The difference between f_2 and f_1 is the bandwidth.

$$\text{Bandwidth} = f_2 - f_1$$

where f_1 = lower cut-off frequency

f_2 = higher cut-off frequency.

Frequency response: The plot drawn between voltage gain and signal frequency of an amplifier is known as frequency response.

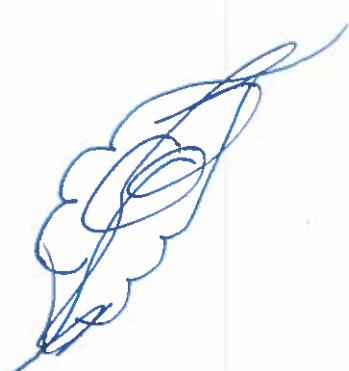


Two stage RC coupled amplifier:

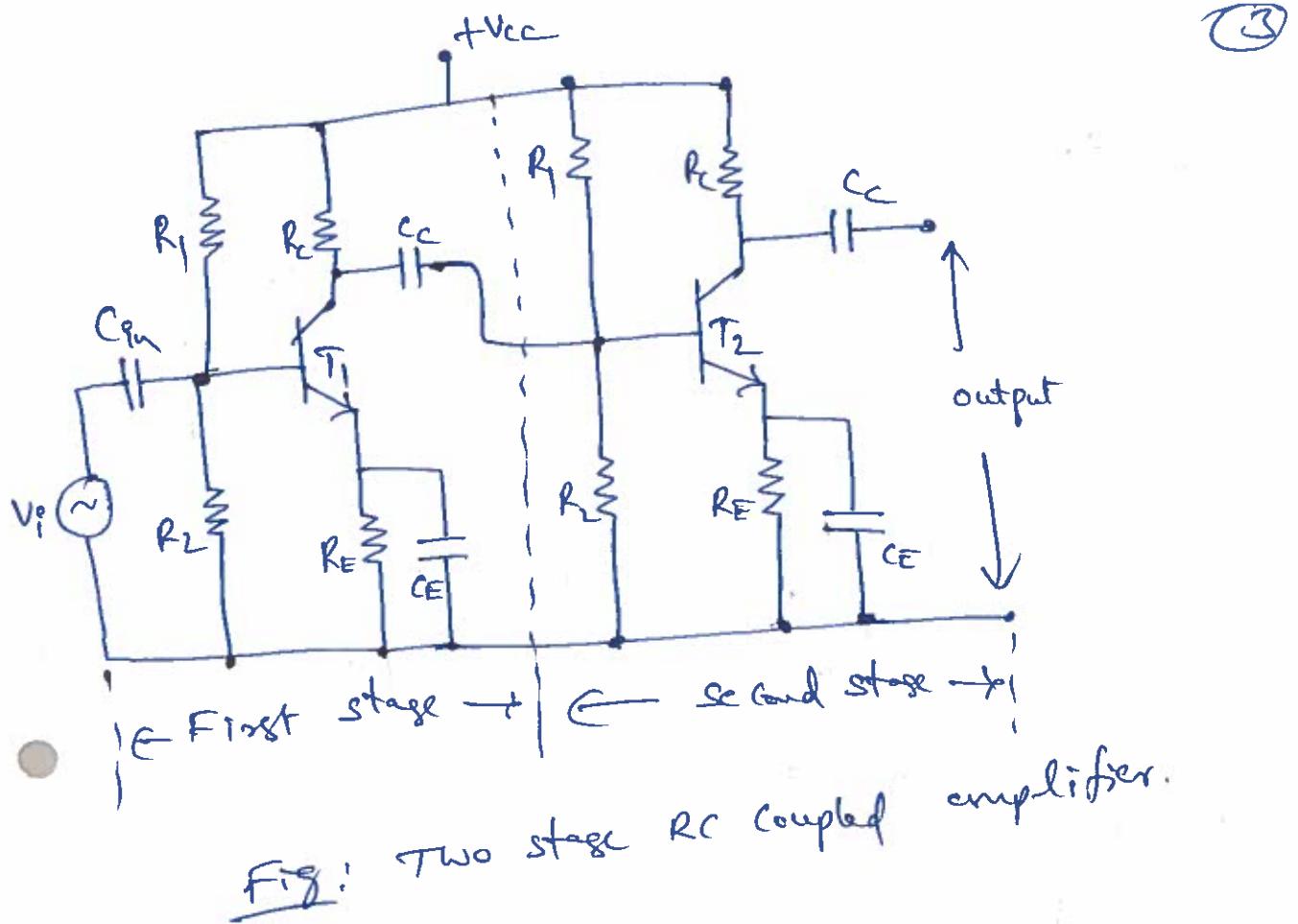
The coupling capacitor C_c connects the output of the first stage to the input of the second stage.

→ The coupling from one stage to the next stage is achieved by coupling capacitor along with a shunt resistor that's why this amplifier is called RC Coupled amplifier.

* ~~The working~~ when the input voltage V_i applied to the base of the first transistor through input capacitor C_{in} , it appears in the amplified form across its collector load R_C . The output of the first stage is given to the base of the next stage through coupling capacitor C_C . The amplified signal of first stage gets further amplification by the second stage and hence more amplification takes place

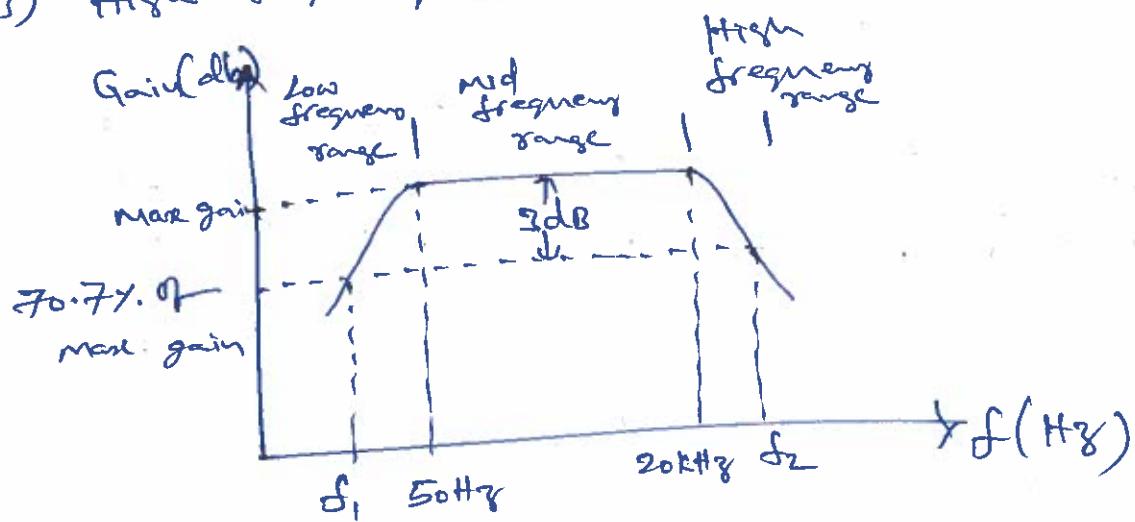


$$\text{Total Gain} = \text{Gain of the first stage} \times \text{Gain of Second stage.}$$



frequency response:

- 1) Low frequency ($< 50\text{Hz}$)
- 2) Mid frequency range ($50\text{Hz} - 20\text{kHz}$)
- 3) High frequency range ($> 20\text{kHz}$)



frequency response of RC coupled amplifier.

Multistage Amplifier (Cascading of Amplifiers)

The gain of the single stage amplifier is insufficient for some applications like TV receivers, communication receivers. requires number of amplification stages may be two or more to increase the gain by the output of each amplifier stage is coupled onto the input of the next stage.

→ An amplifier circuit containing more than one stage of amplification is known as multistage amplifier.

→ The coupling devices are generally capacitors, transformers... used by multistage amplifiers.

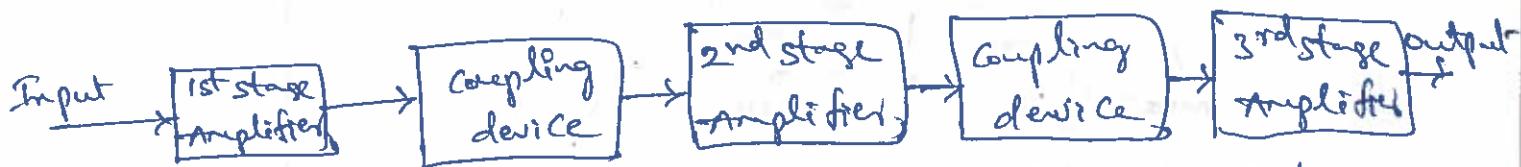


Fig: Diagram of multistage amplifier.

Gain of multistage amplifier:

If A_{V1} , A_{V2} and A_{V3} are the individual stage gains, then overall voltage gain,

$$A_V = A_{V1} \times A_{V2} \times A_{V3}$$